ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 2, March 2013

A Theoretical Study of MOSFET Multi Threshold Voltage over Single Threshold Voltage

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***Abstract:** The paper presents the discussion issues of multi threshold voltage, with single threshold in bulk CMOS technology; the fundamental trends specific to high speed, high complexity systems, power consumption are reviewed, considering the primary issues that constrain existing and future digital and mixed-signal integrated systems. These issues are discussed in terms of the evolving criteria that affect each aspect of the VLSI design and synthesis process. Topics such single threshold and multi threshold voltage CMOS circuits and on-chip interconnect noise, determined by the local nature of the circuit structures, are compared and contrasted with larger issues that focus on the global nature of VLSI-based systems such as synchronization styles and power distribution networks.*

Key words: **Body effect, CMOS technology, Threshold voltage.**

I. INTRODUCTION

Modern chip design has greatly advanced with recent silicon manufacturing technology improvements that escalate transistor counts, increasing a chip's complexity while maintaining its size. This phenomenon will continue, resulting in at least 10 of today's microprocessors fitting onto a single chip by 2005. Consequently design and test of complex digital circuits imposes extreme challenges to current tools and methodologies. VLSI circuit designers are excited by the prospect of addressing these challenges efficiently, but these challenges are becoming increasingly hard to overcome. In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend. Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices which demand high-speed computation and complex functionality with low power consumption.

II. CMOS TECHNOLOGY

For semiconductor integrated circuits, during the past decades, the CMOS technology emerged as the dominant fabrication method, and CMOS became the almost exclusive choice for semiconductor memory designs also. With the development of the CMOS memory technology numerous publications presented select CMOS memory circuit- and architecture-designs, but these disclosures, sometimes for protection of intellectual property, left significant hollows in the acquainted material and made little attempt to provide an unbiased global picture and analysis in an organized form. Furthermore, the analysis, design and improvement of many memory-specific CMOS circuits, e.g. memory cells, array wiring, sense amplifiers, redundant elements, etc., required expertness not only in circuit technology, but also in semiconductor processing and device technologies, modern physics and information theory. The prerequisite for combining these diverse technological and theoretical sciences from disparate sources made the design and the tuition of CMOS memory circuits exceptionally demanding tasks. Additionally, the literature of CMOS technology made little effort to give overview texts and methodical analyses of some significant memory-specific issues such as sense amplifiers, redundancy implementations and radiation hardening by circuit-technical approaches. (1, 2. 3).Since the combination of radiation hardness and high performance was the incipient stimulant to develop CMOS silicon-on-insulator SOI and silicon-on-sapphire SOS memories, this closing chapter devotes a substantial part to the peculiarities of the CMOS SOI (SOS) memory circuit designs. The circuits and architectures presented in this original monograph are specific to CMOS nonprogrammable write-read and read-only memories. Circuits and architectures of programmable memories, e.g. PROMS, EPROMs, EEPROMs, NVROMs and Flash-Memories are not among the subjects of this volume, because during the technical evolution programmable memories have become a separate and extensive category in semiconductor memories. Yet, a multitude of programmable and other semiconductor memory designs can adopt many of the circuits and architectures. As CMOS technology is the basic semiconductor model many of the CMOS techniques are exists and still the revolution is carried out for many of the mixed signal and digital circuitry. The CMOS is the combination of

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 2, March 2013

both PMOS and NMOS, where pull-up network is the PMOS and pull-down network is NMOS is shown from the fig1. This MOSFET works in three regions ie cut-off, linear and saturation region they have given names depending upon the flow of electronics and the applied threshold and gate voltage.(4, 5)

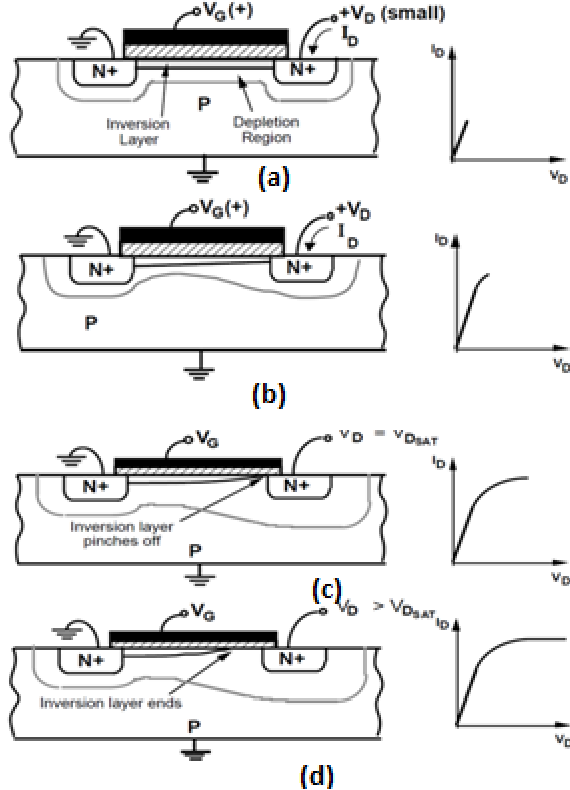

Fig 1 CMOS in 3 different regions and their characteristics (a) cut-off, (b) linear, (c) saturation, (d) saturation in pinch-off condition

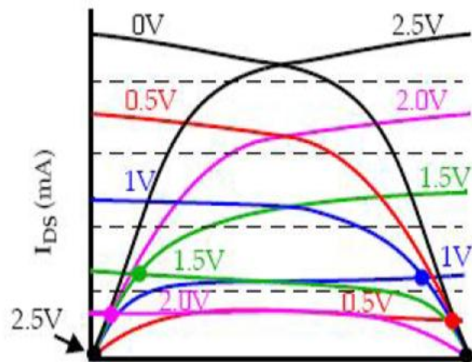

Fig 2 Currents of PMOS and NMOS

Table 1 Relations between voltages for the three regions of operation of CMOS inverter

	Cut-off	Non-saturated	Saturated
P-device	$V_{gsp}>V_{tp}$ $V_{in}>V_{tp}+V_{dd}$	$V_{gsp}<V_{tp}$ $V_{in}<V_{tp}+V_{dd}$	$V_{gsp}<V_{tp}$ $V_{in}<V_{tp}+V_{dd}$

		$V_{dsp}>V_{gsp}-V_{tp}$ $V_{out}>V_{in}-V_{tp}$	$V_{dsp}<V_{gsp}-V_{tp}$ $V_{out}<V_{in}-V_{tp}$
N-device	$V_{gsn}<V_{tn}$ $V_{in}<V_{tn}$	$V_{gsn}>V_{tn}$ $V_{in}>V_{tn}+V_{dd}$ $V_{dsn}<V_{gsn}-V_{tn}$ $V_{out}<V_{in}-V_{tn}$	$V_{gsn}>V_{tn}$ $V_{in}>V_{tn}+V_{dd}$ $V_{dsn}>V_{gsn}-V_{tn}$ $V_{out}>V_{in}-V_{tn}$

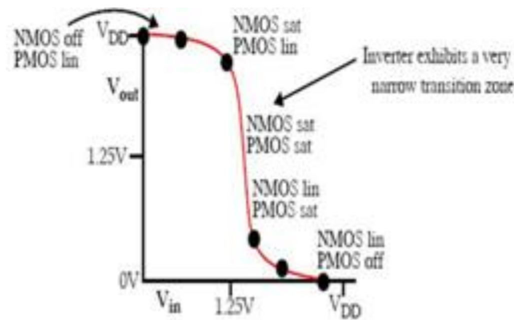

Fig 3 PMOS and NMOS i.e. CMOS working in 3 different regions

A. Definition and Role of Threshold Voltage in Mosfet

The threshold voltage of MOSFETs has traditionally been defined as the gate voltage required causing the surface potential to be equal to twice the Fermi potential in the bulk of semiconductor. MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. The formation of the inversion layer allows the flow of electrons through the gate-source junction (1, 2).Affects of threshold voltage in MOSFET: substrate doping, oxide thickness, source-to-substrate voltage bias, gate material, and surface charge density On the other side threshold voltage can further be said as channel dependent because based on the channel length or channel effects the technology is decided. From past two decades the technology is drastically decreased up to 19nm. Depending up on the technology one can say the fabrication is either short channel or long channel construction. Threshold voltage plays a major role in three different regions and is described briefly in further sections.

B. Threshold Voltage and Body Effect

The threshold voltage V_{th} for a nMOS transistor is the minimum amount of the gate-to-source voltage V_{GS} necessary to cause surface inversion so as to create the conducting channel between the source and the drain. For $V_{GS}< V_{th}$, no current can flow between the source and the drain. For $V_{GS}> V_{th}$, a larger number of minority carriers (electrons in case of an nMOS transistor) are drawn to the surface, increasing the channel current. However, the surface potential and the depletion region width remain almost unchanged as V_{GS} is increased beyond the threshold voltage.(1,2)The physical components determining the threshold voltage are the following.

- Work function difference between the gate and the substrate.
- Gate voltage portion spent to change the surface potential.
- Gate voltage part accounting for the depletion region charge.
- Gate voltage component to offset the fixed charges in the gate oxide and the silicon-oxide boundary.

Although the following analysis pertains to an nMOS device, it can be simply modified to reason for a p-channel device.

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The work function difference ϕ_{GS} between the doped poly-silicon gate and the p-type substrate, which depends on the substrate doping, makes up the first component of the threshold voltage. The externally applied gate voltage must also account for the strong inversion at the surface, expressed in the form of surface potential 2 ϕ_F, where ϕ_F denotes the distance between the intrinsic energy level E_I and the Fermi level E_F of the p-type semiconductor substrate.

The factor 2 comes due to the fact that in the bulk, the semiconductor is p-type, where E_I is above E_F by ϕ_F, while at the inverted n-type region at the surface E_I is below E_F by ϕ_F, and thus the amount of the band bending is 2 ϕ_F . This is the second component of the threshold voltage. The potential difference ϕ_F between E_I and E_F is given as

$$\emptyset_F = KT/q \ln(N_A/n_i) \qquad (1)$$

where k: Boltzmann constant, T: temperature, q : electron charge N_A : acceptor concentration in the p-substrate and n i : intrinsic carrier concentration. The expression kT/q is 0.02586 volt at 300 K.

The applied gate voltage must also be large enough to create the depletion charge. Note that the charge per unit area in the depletion region at strong inversion is given by

$$Q_{do} = -2(\varepsilon_S q N_A \emptyset_F)^{1/2} \qquad (2)$$

where ε_S is the substrate permittivity. If the source is biased at a potential V_{SB} with respect to the substrate, then the depletion charge density is given by

$$Q_d = (-2(\varepsilon_S q N_A(\emptyset_F + V_{SB})))^{1/2} \qquad (3)$$

The component of the threshold voltage that offsets the depletion charge is then given by -Q_d /C_{ox} , where C_{ox} is the gate oxide capacitance per unit area, or C_{ox} = ε_{ox}/t_{ox} (ratio of the oxide permittivity and the oxide thickness).

A set of positive charges arises from the interface states at the Si-SiO_2 interface. These charges, denoted as Q_i , occur from the abrupt termination of the semiconductor crystal lattice at the oxide interface. The component of the gate voltage needed to offset this positive charge (which induces an equivalent negative charge in the semiconductor) is -Q_i /C_{ox}. On combining all the four voltage components, the threshold voltage V_{TO}, for zero substrate bias, is expressed as

$$V_{TO} = \emptyset_{GS} - 2\emptyset_F - \frac{Q_{do}}{C_{ox}} - \frac{Q_i}{C_{ox}} \qquad (4)$$

For non-zero substrate bias, however, the depletion charge density needs to be modified to include the effect of V_{SB} on that charge, resulting in the following generalized expression for the threshold voltage, namely

$$V_t = \emptyset_{GS} - 2\emptyset_F - \frac{Q_{do}}{C_{ox}} - \frac{Q_i}{C_{ox}} \qquad (5)$$

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The generalized form of the threshold voltage can also be written as

$$V_T = \phi_{GS} - 2\phi_F - \frac{Q_{do}}{C_{ox}} - \frac{Q_i}{C_{ox}} - \frac{Q_d - Q_{do}}{C_{ox}} = V_{ro} - \frac{Q_d - Q_{do}}{C_{ox}} \quad (6)$$

Note that the threshold voltage differs from V_{ro} by an additive term due to substrate bias. This term which depends upon material parameter and source to substrate voltage V_{SB} is given by

$$\frac{Q_d - Q_{do}}{C_{ox}} = -\sqrt{\frac{2N_A\varepsilon_{SI}}{C_{ox}}}\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (7)$$

Thus, in its general form, the threshold voltage is determine as

$$V_t = V_{to} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (8)$$

In the parameter γ,known as the substrate bias or body effect and the coefficient is given by

$$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox} \quad (9)$$

The threshold voltage expression is given by (eq 8) can be applied to n channel as well as p channel transistors. However, some of the parameters have opposite polarities for the p MOS and the n MOS transistors. For example the substrate bias voltage, VSB is positive in nMOS and negative for pMOS devices. Also the substrate potential difference ϕ_F is negative in nMOS and positive in pMOS. Whereas, the body effect coefficient γ is

positive in nMOS and negative in pMOS. Typically the threshold voltage of an enhancement mode n channel transistor is positive, while p channel transistor is negative.

(A) Function of V_{th} in Sub-threshold regions

MOS transistor conducts in three regions from the figure(1), here the basic conduction starts with sub-threshold region, this shows that current of an MOSFET transistor occurs when the gate-to-source voltage (V_{GS}) of a transistor is lower than its threshold voltage (V_{TH}). When V_{GS} is larger than V_{TH}, majority carriers are repelled from the gate area of the transistor and a minority carrier channel is created. This is known as *strong-inversion*, as more minority carriers are present in the channel than majority carriers. When V_{GS} is lower than V_{TH}, there are less minority carriers in the channel, but their presence comprises a current and the state is known as *weak-inversion*. In standard CMOS design, this current is a sub-threshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_{TH}, the circuit can be operated using the sub-threshold current with ultra-low power consumption. Fig 1 Weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of V_{TH}, sub-threshold circuits are very sensitive to process variations and temperature fluctuation. Circuit speed improves with increasing I_{on}, therefore it would be desirable to use a small V_t. Can we set V_t at an arbitrarily small value, say 10mV? The answer is no. At $V_{gs}<V_t$, an N-channel MOSFET is in the off-state. However, an undesirable leakage current can flow between the drain and the source. The MOSFET current observed at $V_{gs}<V_t$ is called the **sub-threshold current**. This is the main contributor to the MOSFET off-state current, Ioff. Ioff is the Id measured at $V_{gs}=0$ and $V_{ds}=V_{dd}$. It is important to keep Ioff very small in order to minimize the

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static power that a circuit consumes even when it is in the standby mode. To model the sub-threshold drain current of a MOSFET, model of the electron population density, n(x), under the gate to include a bias between the adjacent n+ region and the channel, i.e. to allow for a non-zero v_{BC},. To understand how this bias, v_{BC}, effects the electron population under the gate, it is instructive to first think about the role the n+ region played in establishing the electron population in the two-terminal MOS capacitor situation We in fact did not even mention the n+ region during derivation, but the n+ region does play a very important role because it supplies the electrons that are under the gate below threshold, i.e., $q_N^*(v_{GB}<V_T)$. The n+ region is a reservoir of electrons, and those electrons spill out of it into the region under the gate when the electrostatic potential energy barrier confining the electrons to the reservoir, -qΔφ, is lowered by a positive gate voltage. The barrier is lowered most near the oxide-silicon interface, and most of the carriers spill across near that interface, however, at any depth that the barrier is reduced, carriers can spill across. What we calculated when we found $qN^*(v_{GB})$ is the total number of electrons that can spill across and into the region under the gate when the voltage on the gate is v_{GB}. If the n+ region is biased positive relative to the substrate, i.e. when $v_{BC} < 0$, then the potential energy of the carriers in the reservoir is lower than when $v_{BC} = 0$ V. As a result fewer carriers can spill out of the source and into the region under the gate; quantitatively, the number that can spill into this region decreases exponentially with $|v_{BC}|$, i.e. e^{v_{BC}/φ_t}.

$$q_N(V_{GB}) = -[n(V_{BC}) - 1]C_{ox}\,\emptyset_t e^{-\frac{[V_t(V_{BC})-V_{oc}]}{n\emptyset_t}} \quad (10)$$

For $V_{GB} < V_T(V_{BC}),\ V_{BC} < 0$

The substrate bias, v_{BC}, does not appear explicitly in Eq. 10, but it does play an important role because now both VT and n are now functions of v_{BC}:

$$n(V_{BC}) = 1 + 1/C_{ox}\sqrt{\varepsilon_{si} q N_a/2[-2\emptyset_p - V_{BC}]} \quad (11)$$

$$V_T(v_{BC}) = V_{FB} + |2\emptyset_p| + |V_{BC}| + 1/C_{ox}\sqrt{2\varepsilon_{si} q N}A(|2\emptyset_p| + |V_{BC}|) \quad (12)$$

When $v_{BC} < 0$, the depletion region is wider near threshold, so n is smaller (near to 1) and the threshold voltage, V_T, is larger than when $v_{BC} = 0$. With the derivation of Eq. 14 it is easy to find the drain current of a MOSFET biased below threshold and in weak inversion, i.e. in the sub-threshold region.

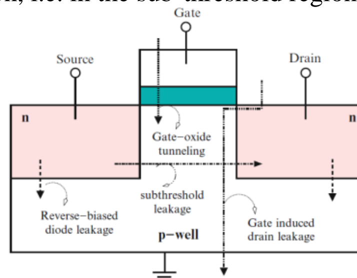

Fig 4 Components of Leakage Power: (i) Sub-threshold current flows between source and drain; (ii) Reverse-biased diode leakage flows across the parasitic diodes; (iii) Gate induced drain leakage flows between the drain and substrate

In the gradual channel approximation modelling of MOSFET terminal characteristics (3) the drain current is identically zero when the gate voltage is less than the threshold voltage, i.e. when $v_{GS} \leq V_T$. As we will soon see, the population of mobile electrons calculated under the gate provides a mechanism for charge flow between the drain and source even when $v_{GS} \leq V_T$, and thus there is in fact a small, non-zero drain current through a MOSFET biased below threshold. This is significant because on an integrated circuit chip with millions of transistors which are supposed to be off and therefore not dissipating any power, a little current flowing through each transistor can easily add up to be a significant power drain, and be a source of serious heating. Furthermore that a MOSFET's characteristics are well defined in the sub-threshold region, and are in no way anomalous or

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ISO 9001:2008 Certified
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parasitic. In fact, they have such interesting properties that it is highly advantageous in a large set of applications to design circuits that operate specifically in the sub-threshold region. (2) Consider the MOSFET, and suppose that it is biased with a positive drain voltage, i.e. $v_{DS} \geq 0$, and a negative substrate voltage, i.e. $v_{BS} \leq 0$. Suppose also that the gate is biased positively and a bit less than threshold. At the source end of the gate, electrons will spill into the region under the gate as the same will be true at the drain end of the gate, and if $v_{DS} = 0$ the electron population under the gate will be uniform because the situation will be equivalent to that in a 3-terminal MOS capacitor, and the steady state current will be identically zero. If $v_{DS} > 0$, however, the density of electrons that can spill under the gate at the drain end will be smaller than at the source end by a factor of e^{-v_{DS}/φ_t}. Rather than electrons flowing under the gate from the drain, the electrons spilling into the region under the gate from the source will flow all the way under the gate and into the drain n+ region when they reach it. As a result there will be a net positive drain current. To calculate the size of this drain current, we need to model how the electrons flow under the gate.(3, 14) First, consider drift. There is a voltage difference between the source and the drain, but the electric field laterally between them is small because the voltage between the back contact and the source, v_{BS}, falls across the depletion region between the n+ source and the p-type substrate, and the voltage between the back (4,5) contact and the drain, v_{BD}, falls across the drain-substrate depletion region. There is thus negligible lateral field in the channel region below threshold to drift any electrons there from source to drain. Recognizing that drift is negligible below threshold, we see that the mechanism behind the sub-threshold drain current must be diffusion driven by the electron concentration gradient going from the source to drain:

$$I_{sub-thr} = I_o * e^{[V_{gs}-V_{th}/nV_T]} * \left(1 - e^{\frac{-V_{Ds}}{V_t}}\right) * e^{\eta V_{Ds}/nV_t} \quad (13)$$

$$I_{sub-thr} = \mu_o C_{ox} W/L(n-1)V_t^2 \quad (14)$$

From the figure 1, 4 shows that MOSFET in sub-threshold region and parameters that effecting in sub-threshold region and the brief description is given ref(2, 3)

(B) Function of V_{Th} in linear region

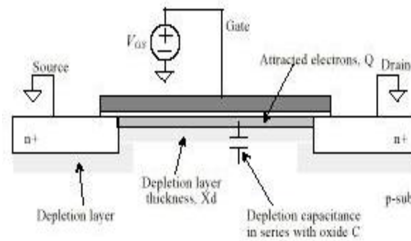

Fig 5 MOS Transistor in linear region

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$

The transistor is turned on, and a channel has been created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as: (8,9)

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad (15)$$

When $V_{GS} > V_{THN}$ (*n* MOSFET), the semiconductor/oxide interface is inverted, i.e., the inversion layer is formed. The associated depletion region (beneath the inversion layer) thickness is described by

$$X_d = \sqrt{2\varepsilon_{si}|\emptyset_s - \emptyset_F|/qN_A} \quad (16)$$

Where $\emptyset_F = -KT/q \ln N_A/n_i$

The charge attracted under the MOS gate is described by

$$Q_b = qN_A X_d = \sqrt{2\varepsilon_{si} qN_A|\emptyset_s - \emptyset_F|}[C/m^2] \quad (17)$$

In accumulation mode, *fs* = *fF* □ □*Qb* ¢ = 0.

When increasing *VGS* (positively) results in *fs* = 0, the semiconductor surface at the oxide interface becomes depleted.

Continuing to increase *VGS* till *fs* =- *fF* results in the formation of the inversion channel.

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Note that the value of *VGS* when *fs* =- *fF* is *VTHN*. In this situation the negative charge in the depletion region is described by

$Q_b = qN_AX_d = \sqrt{2\varepsilon_{si}qN_A|-2\emptyset_F + V_{SB}|}$[C/$m^2$ (18)

Between strong inversion and depletion, *fs* changed a total of 2*fF*.

$$V_{THN} = V_{THNO} + \gamma(\sqrt{|2\emptyset_F|} + \sqrt{V_{SB}} - \sqrt{|2\emptyset_F|}) \quad (19)$$

Where

$$V_{THNO} = -\emptyset_{ms} - 2\emptyset_F + Q_{bo} - Q_{ss}/C_{ox} = V_{FB} - 2\emptyset_F + Q_{bo}/C_{ox} \quad (20)$$

and

$$\gamma = \sqrt{2q\varepsilon_{si}N_A}/C_{ox} \quad (21)$$

The value of *fms* is obtained by adding the contact potentials:

(C)Function of V_{th} in saturation region

When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$

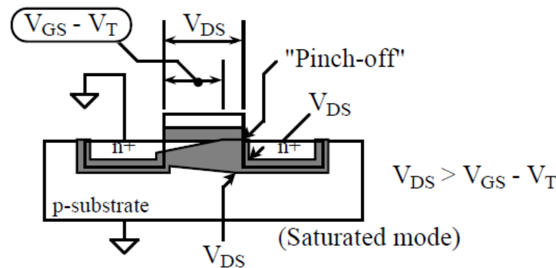

Fig 6 Here the current depends only on VGS and not VDS (if we neglect channel-length modulation) and the channel becomes completely pinched-off near the drain. With VDS > VGS –VT but VS = 0V, then VD > VG - VT and hence, VT > VGD, i.e., Vgate-to-drain is less than the threshold voltage

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as **pinch-off** to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modelled very approximately as: (10, 11)

$$I_D = \mu_n C_{ox} W/2L(V_{GS} - V_{TH})^2(1 + V_{DS}) \quad (22)$$

The additional factor involving λ, the channel-length modulation parameter, models current dependence on drain voltage due to the Early effect, or channel length modulation. According to this equation, a key design parameter, the MOSFET Tran conductance is:

$$g_m = 2I_D/(V_{GS} - V_{TH}) = 2I_D/V_{ov} \quad (23)$$

Where the combination $V_{ov} = V_{GS} - V_{th}$ is called the **overdrive voltage**. Another key design parameter is the MOSFET output resistance given by:

$$r_{out} = -1/I_D \quad (24)$$

r_{ou}t is the inverse of g_{ds} where $g_{DS} =$. V_{DS} is the expression in saturation region.

If λ is taken as zero, an infinite output resistance of the device results that leads to unrealistic circuit predictions, particularly in analog circuits. As the channel length becomes very short, these equations become quite inaccurate. New physical effects arise. For example, carrier transport in the active mode may become limited by velocity saturation. When velocity saturation dominates, the saturation drain current is more nearly linear than

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ISO 9001:2008 Certified
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quadratic in V_{GS}. At even shorter lengths, carriers transport with near zero scattering, known as quasi-ballistic transport. In addition, the output current is affected by drain-induced barrier lowering of the threshold voltage

III. MOSFET WITH MULTIPLE THRESHOLD VOLTAGE

In the above sections, brief description of the threshold voltage is given. In this section the discursion is all about multiple threshold voltage. In past two decades many of the analog and digital circuits is based on the single threshold voltage, which gives in the power consumption, delay and slow in generating output. To overcome these all defects here we introduce a new technique, MOSFET with multiple threshold voltage. Normally to design any VLSI circuit we required MOSFETS to develop. For example a circuit consisting of number of MOSFETS each MOSFET's having with different threshold voltages would be easy to design, and can consume low power with less delays with more efficient and reliable out puts. Many of the low power techniques have come in to existence based on the architecture, design, logics etc but developing the circuits with multiple threshold voltage is one among the low power technique which gives an appropriate results. Multiple threshold voltage CMOS technologies employs both high and low threshold voltage transistor within the same IC. The primary goal of these circuits is to selectively scale the threshold voltages together with the supply voltage in order to enhance the circuit speed without significantly increasing the sub-threshold leakage currents.

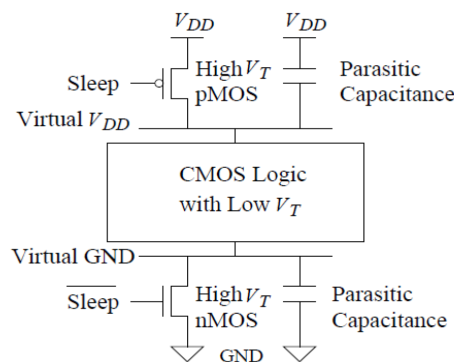

Fig 7 Generic structure of a MTCMOS logic gate

MTCMOS is an enabling technology that provides a high speed performance and low-power operation by utilizing both high and low threshold voltage (V_T) transistors [16,15]. By using low V_T transistors in a signal path, the supply voltage (V_{DD}) can be lowered to reduce the switching power dissipation without affecting the performance. Although the switching power can be reduced quadratic ally according to the V_{DD} reduction, the V_T that has been decreased for the performance compensation incurs an exponential increase in the sub-threshold leakage current. In fact, the increased leakage power can dominate the switching power if the voltage is scaled down aggressively [18, 19]. In many event driven applications, such as a processor running an X-server or a mobile media terminal, circuits are usually in an idle state when no computation is being performed. During this standby state, it is very wasteful to have a large sub-threshold leakage current. This static power dissipation in the standby mode can be reduced dramatically by using high V_T transistors (sleep transistors) with very low leakage currents to gate the power supply. Figure 8 illustrates the basic circuit scheme of the MTCMOS technique. Note that, both the pMOS and nMOS transistors were utilized as sleep transistors as illustrated in Figure 6. However, it has been proved that for a purely combinational logic circuit, the circuit performance (speed) can be increased by employing nMOS transistors alone [15] as illustrated in Figure 7

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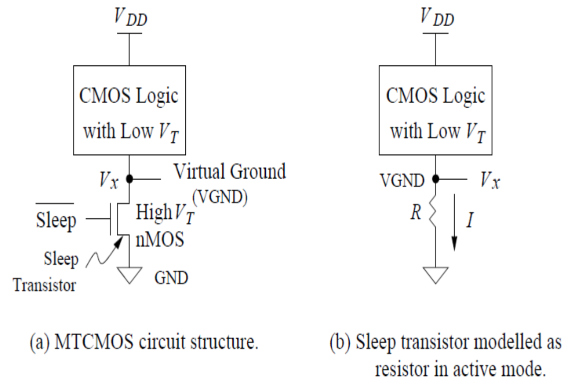

(a) MTCMOS circuit structure. (b) Sleep transistor modelled as resistor in active mode.

Fig 8 Sleep transistor in MTCMOS circuits.

Sleep transistors in MTCMOS circuits are controlled by a \sleep" signal that is used for the active/standby mode control. During the active mode (sleep = 0), the sleep transistor can be approximated by the linear resistor R as seen in Figure 8 (b) [15]. This creates a finite voltage drop (VX = I / R) across the virtual ground nodes as the gates are discharging. This voltage drop causes the internal logic to slow down for two reasons: (i) it reduces the gate's driving capability from V_{DD} to $V_{DD} - V_X$, and, (ii) the internal transistor threshold voltages increase due to the body effect [16]. Therefore, the resistor should be small, and consequently, the size of the sleep transistor should be large. This is, however, a trade off between the circuit speed in the active mode and the standby leakage current, because the total standby leakage current in a chip is proportional to the width of the sleep transistor [17]. As a result, optimal sizing of the sleep transistor for an arbitrary circuit to meet a performance constraint is difficult. In other words, the current \I" owing through the sleep transistor in the active mode needs to achieve the required speed. In the last decade, a number of sleep transistor sizing methodologies have been reported in the literature [15]. The use of a single sleep transistor to support the whole circuit has been proposed in [17]. However, sharing a single sleep transistor for the whole circuit increases the interconnect resistance for the distant blocks. As a result, the sleep transistor has to be sized larger than expected to compensate for the added interconnect resistance. An excessively large size sleep transistor augments the dynamic and leakage power, as well as the area. In order to reduce the area overhead effectively, a hierarchical sizing method, based on the mutual exclusive discharge pattern, was introduced in [16]. The cascaded gates are grouped together by this method, because simultaneous current discharges cannot take place. This method can be efficient for balanced circuits with tree configurations, where mutually exclusive discharging gates are easily detected. However, this method is not efficient for circuits with complicated interconnections and unbalanced structures capability from V_{DD} to $V_{DD} - V_X$, and, (ii) the internal transistor threshold voltages increase due to the body effect [16]. Therefore, the resistor should be small, and consequently, the size of the sleep transistor should be large. This is, however, a trade off between the circuit speed in the active mode and the standby leakage current, because the total standby leakage current in a chip is proportional to the width of the sleep transistor [15]. As a result, optimal sizing of the sleep transistor for an arbitrary circuit to meet a performance constraint is difficult. In other words, the current \I" owing through the sleep transistor in the active mode needs to achieve the required speed. In the last decade, a number of sleep transistor sizing methodologies have been reported in the literature [11, 12]. The use of a single sleep transistor to support the whole circuit has been proposed in [17]. However, sharing a single sleep transistor for the whole circuit increases the interconnect resistance for the distant blocks. As a result, the sleep transistor has to be sized larger than expected to compensate for the added interconnect resistance. An excessively large size sleep transistor augments the dynamic and leakage power, as well as the area. In order to reduce the area overhead effectively, a hierarchical sizing method, based on the mutual exclusive discharge pattern, was introduced in [16]. The cascaded gates are grouped together by this method, because simultaneous current discharges cannot take place. This method can be efficient for balanced circuits with tree configurations, where mutually exclusive discharging gates are easily detected. However, this method is not efficient for circuits with complicated interconnections and unbalanced structures The multiple threshold voltage circuit technique selectively places low threshold voltage on the seed critical paths of a circuit to enhance speed while operating at a reduced supply voltage. In a standard single threshold voltage circuits, the threshold voltage of the transistors are chosen to achieve a specific target clock frequency. Since the speed of

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 2, March 2013

the synchronous digital circuits is determined by the most critical delay paths, the threshold voltages are primarily chosen to lower the propagation delays of the signals along the critical paths in order to satisfy the target clock period (6). A single threshold voltage circuits essentially wastes power in the form of leakage currents on many non critical delay paths. The primary objective of the multiple threshold voltage circuit techniques is to minimize the number of low threshold voltage transistors required to satisfy the target clock frequency while maximizing the high threshold voltage to achieve the lowest sub-threshold leakage currents. The multiple threshold voltage circuit technique provides an opportunity to further scale the threshold voltage without violating any limitations in the total sub-threshold leakage power. A target clock frequency can, therefore, be satisfy with in a limited power by only scaling the threshold voltage of those portions of a circuit where a low threshold voltage transistor is required to achieve in the desire circuit designing.(6,7)
Hence, multiple threshold voltage can either be low or high threshold voltage in the same IC. By obtaining different threshold in the same circuit can reduce leakage currents and can achieve low power. For example to achieve low power, initially considering a circuit with six transistors taking any two transistors with different threshold voltages then calculating the path with same threshold voltages with single clock frequency and then comparing it with (6, 7) another path with different threshold voltages with a single clock frequency, here we can observe that both the paths will suffer with leakage currents if it is in standby mode but the path with different threshold voltage can acquire low leakage currents and can operate with low power, these all can be shown theoretically and practically

IV. CONCULSION

The primary goal of the paper is to give a brief theoretical description of MOSFET multi threshold voltage with single threshold. After studying the various circuit issues of the MOSFET, threshold voltage plays a major role in conducting device which gives appropriate VI characteristics. And finally the paper gives superiority issues of the multi threshold voltage over single threshold and the parameters that include in both the circuit designs and its superiority is demonstrated.

REFERENCES

[1] J Neil H. E. Weste, David Harris, and Ayan Banerjee, CMOS VLSI Design: A circuits and system perspective (3rd edition), Pearson education, 2008.

[2] LESSONS IN ELECTRIC CIRCUITS” Volume three-semiconductors Fifth Edition, last update July 02, 2007.

[3] K. Roy, S. Mukhopadhyay, H. Mahmoodi-Meimand, “Leakage Current Mechanisms and Leakage Reduction Techniques in Deep- Sub micrometer CMOS Circuits”. Proceedings of the IEEE, Volume: 91, Issue: 2 On Page(s): 305 - 327 Product Type: Journals & Magazines Feb.2003.

[4] D. Rairigh, “Limits of CMOS technology scaling and technologies beyond-CMOS,” Student Member of IEEE, 2006.

[5] Mizuno T et al. Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFETs. IEEE Transactions on Electron Devices 1994; 41(11):2216–2221.

[6] Multi-voltage CMOS Circuit Design By Volkan Kursun, Eby G. Friedman.

[7] Multi-Threshold Cmos Digital Circuits: Managing Leakage Power By Mohab Anis, Mohamed I. Elmasr.

[8] SUNG-MO KANG AND YUSUF LEBLEBICI, CMOS Digital Integrated Circuits - Analysis and Design, McGraw-Hill, 2003.

[9] KAUSHIK ROY SHARAT PRASAD “Low Power CMOS VLSI Circuit Design” by John Wiley 2000.

[10] D. Rairigh, “Limits of CMOS technology scaling and technologies beyond-CMOS,” IEEE, 2006.

[11] F. Silveria, D. Flandre, P. G. A. Jespers, “A gm/ID Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micro power OTA,” IEEE J. Sol. St. Ckts, 31(9), 1314-1319(1996).

[12] S. Kang and Y. Leblebici, CMOS Digital Integrated Circuits, McGraw-Hill, New York, 2003.

[13] J. Kao and A. Chandrakasan, \MTCMOS Sequential Circuits," In Proceedings of the 27th European Solid State Circuits Conference, pp. 861{869, 2001.

[14] J. Kao, S. Narendra, and A. Chandrakasan, \Sub threshold Leakage Modeling and Reduction Techniques," In Proceedings of the International Conference on Computer Aided Design, pp. 141{148, 2002.

ISSN: 2319-5967
ISO 9001:2008 Certified
International Journal of Engineering Science and Innovative Technology (IJESIT)
Volume 2, Issue 2, March 2013

[15] J. Kao, A. Chandrakasan, and D. Antoniadis, \Transistor Sizing Issues and Tools for Multi-threshold CMOS Technology," In Proceedings of the 34th Design Automation Conference, pp. 409{414, Las Vegas, Nevada, 1997.

[16] J. Kao, S. Narendra, and A. Chandrakasan, \MTCMOS Hierarchical Sizing Based on Mutual Exclusive Discharge Patterns," In Proceedings of the 35th Design Automation Conference, pp. 495{500, Las Vegas, Nevada, 1998.

[17] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, \1-V Power Supply High-Speed Digital Circuit Technology with Multi-Threshold Voltage CMOS," IEEE Journal of Solid-State Circuits, vol. 30, No. 8, pp. 847{854, 1995.

[18] J. M. Rabaey, Digital Integrated Circuits, Prentice Hall, NJ, 1996.

[19] A. Chandrakasan, I. Yang, C. Vieri, and D. Antoniadis, \Design Considerations and Tools for Low-Voltage Digital System Design," In Proceedings of the 33rd Design Automation Conference, pp. 113{118, 1996.